Physical Architectures for Packet-Switching Network Nodes Based on Nonlinear Logic Gates

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***Abstract*—Two new architectures are proposed for designing physical network nodes in packet-switched structures. They allow transparent optical packet networking and are based on the association of various subsystems, which have previously been proposed, and demonstrated. These elements are mainly based on the application of nonlinear behavior in semiconductor optical amplifiers.**

I. INTRODUCTION

Transparent optical networking and packet-switching represents two main ingredients required for the optimization of the performance of optical network in terms of throughput and connectivity. They could constitute a major breakthrough in the evolution of networks for application such as new interactive Internet, massive parallel processing, massive data storage, etc. The former concept has greatly progressed in the past few years in the frame of circuit switching based on add-and-drop multiplexing and optical-cross connects. On the other hand, packet-switching [1] is not yet a mature technology due to difficulty in performing optical logics and developing optical buffers. Many proposals and demonstration of all-optical logic element dedicated to packet-switching applications have been presented in the past years in order to progress toward this objective.

This presentation describes two new switching node architectures making use of such elements, which were developed within our own laboratories.

In packet-switching, the packets are steered towards their destinations by interrogating their destination address encoded in their header (which will be called "label" in this paper as a reference to the MPLS protocol). The packet label must be separated, recognized and possibly rewritten in every core router. This can be time consuming given that core routers must forward millions of packets per second. As most of core routers in backbone or metro networks have only four to eight outgoing ports, it may be possible to determine a packet's engress port by looking at only a small subset of the label bits in the destination address and thus the cost and complexity of individual components of the all optical label switching node can be reduced.

The physical label coding scheme and the related label recognition method constitute the main characteristics of the switching architecture. The bit-serial approach is used in the packet-switching architectures described in this article. In this scheme both the label and the payload are modulated using the same format and bit-rate in order to simplify the emission hardware and software. This reduces not only the packet format complexity, but also the label duration (leading to a greater effective data rate). This coding is then associated with a slowed-down label processing method, which, allows treatment of high bit-rate labels and, in opposition to bit pattern matching methods (using XOR gates), do not require a local generation of the label bit-patterns for comparison.

The two architectures proposed are an optoelectronic one, which uses moderate-speed photo-detectors and electronics, and an all-optical one, which requires a new sub-system concept, i.e. an optical decoder, and a new self-routing technique in order to eliminate the need for an optical address lookup table. These schemes are illustrated on figure 1 and 4. They both use a time-to-wavelength converter in order to perform the series-to-parallel "slowing down" operation. This element is described in part II.

Other common sub-systems to both schemes are the packet pulse extractor, which generates a single pulse indicating to the other switch element the precise arrival time of the label and the spatial switch, which we have depicted as a wavelength converter (and have not been specifically studied).

II. OPTOELECTRONIC PACKET SWITCHING SYSTEM

Figure 1 illustrates the optoelectronic proposal for the packet-switching node architecture which includes three main sub-systems: synchronization & buffering, label extraction & processing, and packet forwarding. We can note that this scheme can be easily adapted to photonic slot routing [2].

A. Synchronization & buffering

The synchronization & buffering subsystem conserves the packet payload information in the optical domain during the processing and packet routing operations performed on the packet label. Moreover, it is responsible for timing and synchronizing the different subsystems.

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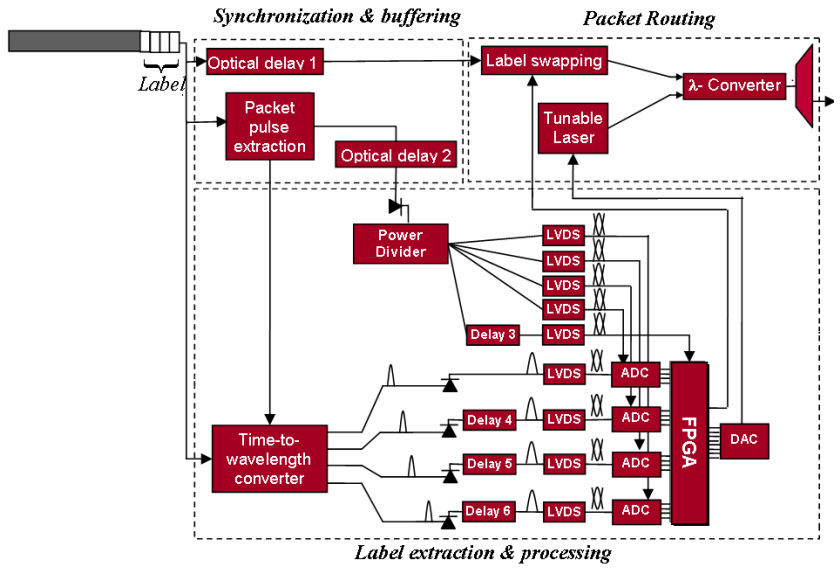

Figure 1- Schematic diagram of the proposed optoelectronic packet-switching system

In our design, a true clock-recovery is not an absolute requirement. Only the beginning of each packet must be known. Provided a marker pulse identifies the beginning of the packet, the other label treatment sub-systems can be triggered at the right moment. A packet pulse extractor sub-system including a packet clock-recovery circuit and an optical AND-gate [4] has been previously proposed by the authors and will be described during the presentation.

A fiber delay line (FDL) is a simple solution for static optical buffering through which the departing times of packets are time-shifted. However, they can only provide limited buffer capacity and coarse delay granularity due to the bulky size of FDL [5]. Slow-light techniques are also proposed for precise synchronizations [6].

B. Label extraction & processing

The basic idea relies on time-to-wavelength conversion whereby a subset of a packet label is distributed onto distinct wavelengths (serial-to-parallel conversion). The parallelized bits are processed within a subsystem in order to deliver the proper command signals to the optical payload switch and to the label swapping subsystem.

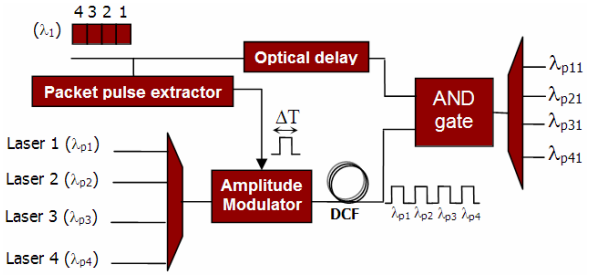

Figure 2- Schematic diagram of a 4-bit time-to-wavelength converter

A 4-bit time-to-wavelength converter based on the four wave mixing (FWM) effect in a SOA has been demonstrated in an earlier experiment at 10Gbit/s (Fig. 2) [7]. Fig. 3 represents the results when a data sequence (probe) at λ=1553.1 nm is launched together with 4 auxiliary modulated beams (pumps) at λ=1551.4 nm, 1550.95 nm, 1550.15 nm and 1549.35 nm. The extinction ratio is between 9 dB and 12.5 dB. A time-to-wavelength converter, with enhanced polarization insensitivity, has also been demonstrated at 10 Gbit/s [7]. This setup is easily modified in order to cope with higher bit rates.

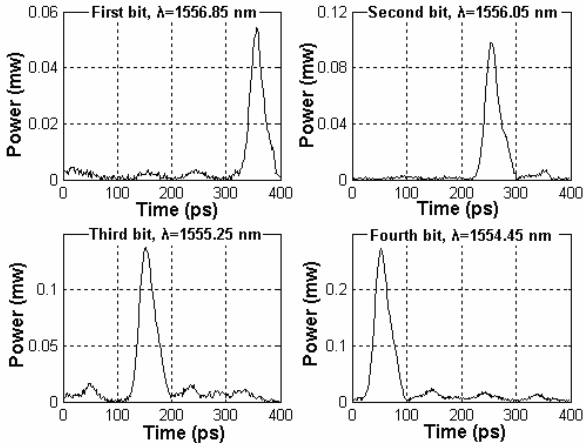

Figure 3- Four wavelength-separated bits at the output of the final demultiplexer

By means of four photo-detectors, the parallelized bits are converted into electrical format. Next, they are transformed into the LVDS (Low Voltage Differential Signaling) format before processing. An 8-bit Analog Devices AD9480 analog-to-digital converter (ADC) optimized for a 250 MSPS conversion rate is used for sampling, amplifying and buffering the electrical signal as well as producing a varying detection threshold level.

If the routing table is fixed, one can use a logic circuit to produce the required command signal. In dynamic routing, an adaptive algorithm must be performed. The only cost effective and power efficient solution is using an FPGA. The electronic command signal delivered by the label processing subsystem is used to control the spatial

switch. Different electrical voltage levels can be assigned for different label bit combinations. A digital-to-analog converter can be used for providing the required voltages.

C. *Packet forwarding*

The packet label-swapping, together with the optical-switching, constitutes the forwarding operation. Optical switching can be performed using different technologies based on space, time, wavelength, or code diversity. Here, the packet forwarding is based on wavelength switching whereby the output wavelength is chosen based on the processed label subset. An arrayed waveguide grating (AWG) wavelength demultiplexer can be used in order to provide spatial switching of the packet at the output of the system. Wavelength-based optical switches can be designed in numerous ways. The most straightforward is to incorporate a tunable laser and a wavelength converter. Optical wavelength converters that utilize nonlinearities in SOAs offer some advantages in terms of integration potential, power consumption, and optical power efficiency [8].

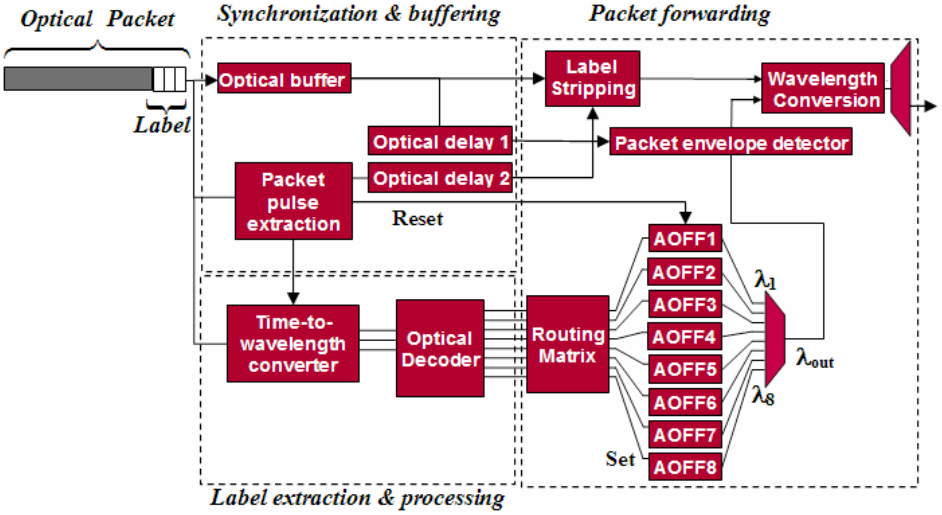

Figure 4- Schematic representation of an all-optical packet switching system

III. ALL-OPTICAL PACKET SWITCHING SYSTEM

Fig. 4 is a schematic representation of the proposed architecture. The synchronization & buffering subsystem is similar to that of part II. The other subsystems are described in the following sections.

A. *Label extraction & processing*

Following the time-to-wavelength converter, the parallelized bits are amplified and sent toward an optical decoder module which produces an optical command pulse corresponding to each label subset combination. A decoder consists in combinational circuits that convert binary information from n-bit coded inputs to 2n unique outputs. The demonstration of an all-optical 3×8 decoder based on the Cross-polarization Modulation (XPolM) in an SOA at 10 Gbit/s is presented in [9]. The measured extinction ratio of the output signals is between 7.9 dB and 12 dB. The design requires only one active optical device per output.

The decoder output bit error rate is 10^{-7} on '1' and 10^{-8} on '0' bits (PRBS $2^{15}-1$) leading to an effective bit-error-rate of 2.2×10^{-8} which could be improved with a finer selection of the non linear devices.

B. *Packet forwarding*

The packet forwarding system includes the adaptive wavelength selection, the packet envelope detection, the label stripping and the wavelength conversion. All-optical flip-flops can be employed in order to provide an all-optical wavelength selection system [10]. The switching time, the required power of the set and reset pulses used to switch the device and the over-all system integration are the main parameters of the optical flip-flops [3]. Each flip-flop has two output wavelengths namely, λ_{ON} and λ_{OFF}. In the present experiment, all the λ_{OFF} are identical (e.g. λ_0). It will be filtered out by the multiplexer. Eight distinct wavelengths ($\lambda_1, \cdots, \lambda_8$) are chosen for 8 flip-flops' λ_{ON}. In the first step, all of the flip-flops are reset by the packet pulse extraction signal. When the decoder output pulse passes through the routing matrix, it sets the associated optical flip-flop. Finally, the selected wavelength (λ_{ON}) is launched into the proper input of the multiplexer so as to exit through the pigtailed output. The set and reset pulse-widths are important in this design, which depends on the all-optical flip-flop technology. When the label bits are modulated in RZ format, the set and reset pulse-widths (e.g. ~10 ps for 40 Gbit/s rates) may be too small for driving (switching) the flip-flops. Pulse width [11] and RZ to NRZ conversions [12] are some of the techniques proposed for all-optical pulse broadening.

Recently, new labeling methods have been proposed whereby new label generation for label swapping at intermediate nodes is not required [13]. The packet end-to-end label consists of multiple local labels. In each intermediate node, a part of this label is stripped off and a switching decision is made. This procedure is repeated up to the end of the destination network node. The architecture presented is based on this idea.

IV. DISCUSSION

Both the packet switching systems presented in this paper and illustrated in Fig. 1 and 4 are transparent for the packet payload. The presented schemes have many other benefits including:

• Packet rate scalability: Due to the payload transparency, its data rate can be considered only at the level of the final wavelength-conversion. The only modification required in order to tune the operation rate of time-to-wavelength converter is to reduce the dispersion of the dispersive element or the wavelength spacing of the lasers and to increase the pulse modulation speed.

• Asynchronous mode operation: The proposed time-to-wavelength converter as well as the other subsystems only needs a single timing information specifying the time of arrival of the label in order to operate properly. This timing information is delivered internally by the packet pulse extractor.

• Modularity: The design and the optimization of each subsystem can be done independently.

• Flexibility: By increasing the order of the time-to-wavelength converter, the length of the label subset processed may be increased. FWM conversion efficiency for larger wavelength detunings may become critical. Dual pump based FWM methods can be used in order to overcome this problem. On the other hand, the all-optical decoder does not seem to be able to cope with a larger number of bits to process. The optoelectronic solution may be better for such cases.

• Polarization diversity: As the input packet polarization state is unknown, using FWM or XPolM in the time-to-wavelength converter or the optical decoder may become problematic. A solution consists in inserting a polarization insensitive wavelength converter such as the one presented in [14] in order to set the operational polarization to the desired state.

V. CONCLUSION

The design and the partial implementation of a packet routing system are demonstrated in this article. Two solutions are presented based respectively on an optoelectronic architecture and an all-optical one. In these architectures, a label subset is processed in order to route the packet. A time-to-wavelength converter is employed as a serial-to-parallel converter. The slowed-down parallelized label bits are processed either via an electronic subsystem or within an all-optical decoder. The main advantage of these approaches is the ability to route the packets or bursts independently of packet length.

Asynchronous mode functionality of the proposed packet label processing module depends directly on the performance of the pulse packet extraction sub-system. Optical integration of the subsystems appears to be possible and will be valuable for reducing cost and enhancing flexibility.

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